REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-5, 7-14, and 18-20 are pending in this application. Claims 6 and 15-17 are canceled without prejudice and new claims 18-20 are added. Claims 1, 7, and 8 are amended by the present response. No new matter is believed to be added.

Claims 1-17 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 4,817,052 to Shinoda et al. (herein "Shinoda"). That rejection is traversed by the present response as discussed next.

Independent claim 1 as now written is directed to a semiconductor memory device including a memory cell array including at least a first area and a second area. A data input circuit is located closer to the first area than the second area, to which cell data stored in the memory cell array is input. An error correction circuit generates parity data for error correction from the cell data input to the data input circuit. A control circuit writes the parity data into the first area and writes the second data into the second area at a time of a writing operation.

The claimed structure allows a semiconductor device of the present invention to utilize an error correcting code (ECC) circuit to separately write data to be written, i.e. write data that requires more time to be written, into a memory area closer to an input/output circuit, and to write data that requires less time to be written into a further memory, thereby making it possible to decrease the total time required for data to be written.

More specifically, and with reference to Figure 1 in the present specification as a non-limiting example, the claimed invention can operate to (a) divide data during a writing operation, for example dividing 32-bit cell data (input/output data) into first 19-bit data that includes 6-bit parity data and second 19-bit data that does not include parity bits, (b) activate a first memory area (for example area MA6) closer to an input/output circuit and a second

memory area (for example area MA0) further from the input/output circuit substantially simultaneously, and (c) write the second data, which requires a shorter data writing time than the first data, into the second further memory area. Writing data into the second memory area incurs a wiring delay time resulting from the greater distance to the second memory area, and writing the first data in the first memory area requires a longer data writing time than the second data as a result of the time needed to generate the priority data, but in writing into the first memory area a wiring delay time is decreased by the nearness to the first memory area.

The present invention can be particularly beneficial when a switching circuit is provided between a first data line connected to a first memory area and a second data line connected to a second memory area such that the second data line is selectively activated, and thereby a part of an electrical power consumed by the data lines can be eliminated. Thereby, the present invention can be highly effective in decreasing power consumption.

The claims as written are believed to clearly distinguish over Shinoda.

The outstanding rejection relies on Shinoda to disclose a memory array of elements M-ARY1, M-ARY2, M-ARY3, and M-ARY4, a data input circuit DOB, an error correction circuit ECC, and a control circuit control CKT.

In reply to the outstanding rejection, applicants first note in the claims the memory cell array includes a first area and a second area, and parity data is written into the first area. That is, in the claims parity data is written into the first area of the memory cell array. For Shinoda to meet that limitation, Shinoda would have to operate such that parity data is written into one area of the memory cell array's M-ARY1, M-ARY2, M-ARY3, and M-ARY4. Shinoda does not operate in that manner, as even recognized in the Office Action. Specifically, the Office Action recognizes that in Shinoda parity data is not stored in any of the noted memory arrays. Shinoda merely discloses storing parity data and cell data in different areas, but again as noted above not in different areas of the same memory cell array.

Further, Shinoda does not disclose or suggest a structure of separately writing data in a memory area closer to an input/output circuit.

As noted above, with the claimed invention a structure can be realized in which data that requires much time to be written (for example which includes priority data) is written in a memory area closer to an input/output circuit, and data that does not require much time to be written is written into a further memory area. In the claimed invention the parity data is written into the first area, which is closer to the input circuit than the second area. Shinoda does not disclose or suggest any structure in which parity data would be written into a first closer area of a memory cell array.

In view of the foregoing comments, the claims as written are believed to clearly distinguish over Shinoda.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Surinder Sachar
Registration No. 34,423

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

EHK/SNS/law

I:\ATTY\SNS\25s\251862\251862US-AM.DOC